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An 8-Bit Flash Analog to Digital Convertor

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ABSTRACT:
Need constantly exists for converters with higher resolution, faster conversion speed and lower power dissipation. High-speed analog to digital converters (ADC's) have been based on flash architecture, because all comparators sample the analog input voltage simultaneously, this ADC is thus inherently fast. Unfortunately, flash ADC requires 2^{N-1} comparators to convert N bit digital code from an analog sample. This makes flash ADC's unsuitable for high-resolution applications. This paper demonstrates a simple technique to reduce comparator requirement of 8-bit flash ADC that requires as few as 128 comparators for 8-bit conversion. In this approach, the analog input range is partitioned into 128 quantization cells, separated by 127 boundary points. A 7-bit binary code 0000000 to 1111111 is assigned to each cell. A 8-bit flash converter requires 256 comparators, while proposed technique reduces number of comparator requirements to 128 for 8-bit conversion.

KEYWORDS: *Flash ADC; µP; DAC; Sample and Hold; Successive Approximation*

I. INTRODUCTION

Analog-to-digital converters (ADCs) are critical building blocks in a wide range of hardware from radar and electronic warfare systems to multimedia based personal computers and work stations [1]. The need constantly exists for converters with higher resolution, faster conversion speeds and lower power dissipation. An N-bit flash architecture uses 2N-1 comparators, where N is the stated resolution. Flash converters often include one or two additional comparators to measure overflow conditions [2]. All comparators sample the analog input voltage simultaneously. This ADC is thus inherently fast. The Parallelism of the flash architecture has drawbacks for higher resolution applications. The number of comparators grows exponentially with N, in addition, the separation of adjacent reference voltages grows smaller exponentially, and consequently this architecture requires very large IC's. It has high power dissipation. Two step Flash converters are popular for conversion resolutions in the 8-12 bit range where optimized designs can achieve low power dissipation and small silicon area for implementation [3],[4]. However, beyond such resolution, the area and power dissipation of two-step Flash ADC's nearly double for each additional bit of resolution [5]. Typically high-resolution ADC's have been based either on self-calibrated successive approximation [6],[7] or over sampling architectures [8], [9]. But both of these architectures are unsuitable for high speed applications. There are many different architectures like pipelined convertor [10], [11], successive approximation convertor [12], [13], Sigma-Delta convertor [14], folding ADC's [15], reported recently for high speed applications. But these architectures have significant amount of complexity. In this paper an 8-bit Architecture of analog to digital (ADC) converter is proposed to improve the sampling rate of an ADC. The prototype ADC based on this technique uses only 128 comparators instead of 256 comparators normally required in the conventional parallel ADCs for 8-bit resolution. This reduces to requirement of comparators by 50%.

II. ADC ARCHITECTURE

The block diagram of the proposed 8-bit ADC is illustrated in Fig. 1. It is based on a successive approximation technique. The ADC consists of an input sample and hold amplifier (SHA), 7-bit flash ADC, 8-bit DAC, 8-bit µP 8085 and some extra supporting circuit blocks. 7-bit flash ADC partitions input range into 127-quantization cells. From the 7- bit code, µP 8085 decides within which cell the input sample lies. This gives 7 bits 0000000 to 111111 according to the cell value. Remaining LSB bit is obtained by successive approximation technique. A binary count is loaded into the Register A depending on the 7-bit code. The detailed binary count to be loaded for different code is summarized in table- I. The analog to digital converter is designed and developed using µP 8085. The 7-bit code generated by 7-bit flash ADC is fed to Port A of 8255. Depending on the code value, a binary count is loaded in Register A as given in table-I. The successive approximation technique is used to get a final 8-bit digital code for the analog input signal.

TABLE I 8-BIT COUNT CORRESPONDING TO 7-BIT FLASH ADC CODE

Sl. No.	Output of 7-bit Flash ADC	Count to be loaded in Accumulator
1	0000000	00000001
2	0000001	00000011
3	0000010	00000101
4	0000011	00000111
5	0000100	00001001
6	0000101	00001011
7	0000110	00001101
10	0000111	00001111
11	0001000	00010001
12	0001001	00010011
13	0001010	00010101
14	0001011	00010111
15	0001100	00011001
16	0001101	00011011
17	0001110	00011101
18	0001111	00011111
19	0010000	00100001
20	0010001	00100011
21	0010010	00100101
22	0010011	00100111
23	0010100	00101001
24	0010101	00101011
25	0010110	00101101
|	|	|
|	|	|
|	|	|
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|	|	|
|	|	|
|	|	|
|	|	|
124	1111100	11111001
125	1111101	11111011
126	1111110	11111101
127	1111111	11111111

III. CIRCUIT IMPLEMENTATION

The block diagram of the 8-bit ADC is as shown in Fig. 1. The 8255 port A is used as input port which gets the 7-bit code from Flash ADC. Corresponding 8-bit binary code is loaded into the accumulator as in the table-1. Port B is used as output port, connected to 8-bit DAC to obtain analog signal equivalent to digital count in Register A, which is compared with an analog input voltage V_{IN}. Equivalent 8- bit digital code for analog input signal is obtained by successive approximation technique.

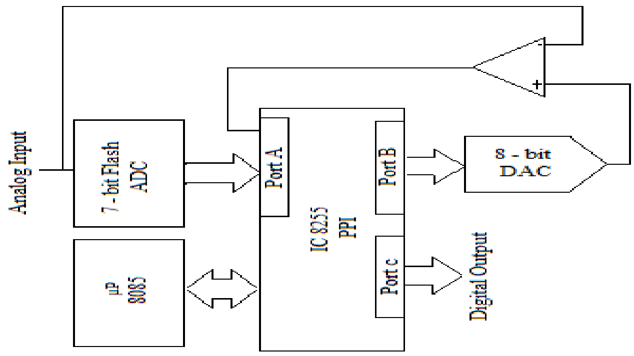

Fig. 1 Block Diagram of 8-bit ADC

The conversion algorithm is similar to the binary search algorithm. First, the reference voltage of a particular cell, Vref (DAC) provided by DAC is set to V_N / 2 to obtain the MSB, where V_N is the maximum cell voltage of a particular cell and N is cell number. After getting the MSB, successive approximation convertor moves to the next bit with $V_N/4$ or $3/4*V_N$ depending on the result of the MSB. If the MSB is “1", then Vref(DAC) = ¾*V_N, otherwise Vref(DAC) =$V_N/4$. This sequence will continue until the LSB is obtained. After completion of two comparisons, count in the Register A is digital equivalent of Analog input voltage V_{IN}. To get an 8-bit digital output, only one comparison is needed, while it is 8 comparisons in the normal successive approximation ADC. Finally 8-bit digital code is available at port C. Software for implementing successive approximation converter in µP8085 is written in assembler code.

IV. MEASURED RESULT

An experimental prototype of 8-bit ADC using proposed technique was designed and developed using µP8085. The working functionality of the ADC has been checked by generating a ramp input going from 0 to 3.5V (full scale range of the ADC). Digital codes have been obtained correctly, going from 0 to 255 for 8-bit at the output, indicating that the ADC working is functionally correct. Both the differential and integral nonlinearities (DNL and INL) were measured over 2^8 output codes by applying slowly varying full scale range ramp as input to the proposed ADC, which completes the full scale range in 255 steps .The values of the each code are compared with ideal value and store the difference value. The results show that the ADC exhibits a Maximum DNL of 0.49LSB and a maximum INL of 0.48LSB as shown in the Fig. 2(a) and 2(b)

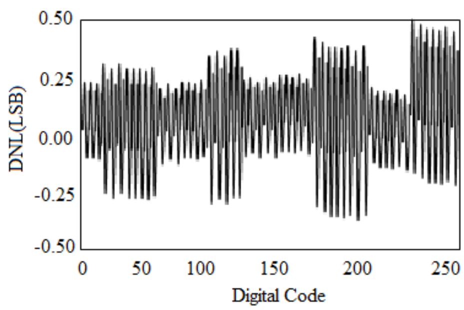

Fig. 2(a) DNL Versus output Code

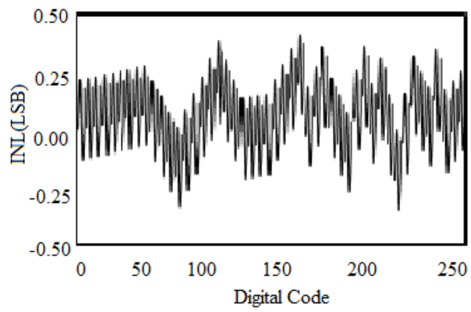

Fig. 2(b) INL Versus output Code

V. CONCLUSIONS

We have presented a simple and effective technique to reduce comparator requirement of 8- bit flash ADC that require as few as 128 comparators for 8-bit conversion.This technique would be effective in a large number of high speed controls and signal processing applications such as hard-disk-drive read Chanel and wireless receivers. Although these applications are most often implemented with Flash convertors, but these ADC's demands larger power. Also, the ADC die area and power dissipation increase exponentially with resolution, limiting the resolution of such ADC's less than 10-bits. This paper shows that partitioning analog input range increases the conversion rate of successive approximation ADC's. The main conclusion is that although Flash convertors provide high conversion rates, required power dissipation of these ADC's are large. Also, resolution beyond 10-bits these ADC's become prohibitively expensive and bulky. Proposed technique provides high enough conversion speed for high speed applications, with less power dissipation even beyond 10-bit resolution. Implementation of successive approximation algorithm in Microprocessor has reduced the hardware requirement and cost. Proposed technique uses only 128 comparators for 8-bit conversion. Hence 50% of comparator requirement is reduced in this technique.

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